ISSN: 2277-9655
(I2OR), Publication Impact Factor: 3.785

IJESRT

INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY

SOFT COMPUTING STUDY OF HYBRID CMOS-SET MADE NIBBLE MULTIPLEXER FOR ADVANCED DIGITAL COMPUTATIONS

Dr. Jayanta Gope (MIEEE) *, & Deep Mukherjee, Arijeet Kushari, Mahuya Panda
Dept. of ECE, Camellia School of Engg. and Tech., WBUT, Barasat, Kolkata-700124, India
Dept. of ECE, Camellia School of Engg. and Tech., WBUT, Barasat, Kolkata-700124, India
Dept. of ECE, Camellia School of Engg. and Tech., WBUT, Barasat, Kolkata-700124, India
Dept. of EE, Camellia School of Engg. and Tech., WBUT, Barasat, Kolkata-700124, India

ABSTRACT

Nibble Multiplexers are one of the specific requisites of modern engineering. Here, authors have attempted to design noble hybrid CMOS-SET made Mahapatra-Ionesco-Banerjee (MIB) based Nibble Multiplexers. The designed model is simulated using BSIM 4.0 and in the subsequent section it is compared with CMOS made nibble multiplexer. The design shows greater figure of merit and thereby enhances the acceptability of such circuit in future electronics.

KEYWORDS: CMOS, Hybrid CMOS-SET, MIB Model, Nibble Multiplexer, SET.

INTRODUCTION

Device physics matured in the late 90s empowering scaling down technology of CMOS made transistors [1]. It was governed by Moore's law and off late ITRS 2005 [2] significantly pronounced the death of CMOS technology owing to its architectural limitation. Researchers then bestowed upon in dwindling down the device size in nanometer region by incorporating Single Electron Transistor technology & apparently emphasized in designing Single Electron Transistor (SET) made devices [3-8]. But the fragility is the SETs lacks in producing high gain & Categorically Cannot be fabricated in room temperature operations thereby producing significant background charge. On the other hand, CMOS has been studied long enough and it possess the virtue of high gain as well as it can be fabricated for massive production in room temperature. But the catastrophic demerit of CMOS is its technological limitations due to the minimum allowable channel length, depth offset thickness, volatility, tenderness and leakage power. This is why scientists in Delft University mobilized both SET and CMOS to amalgamate them to design hybrid CMOS SET structure and studied its performance. Then after, MIB model was deliberated by Professor Shantanu Mahapatra and his team of co-researchers which inspired innumerous pathways in device research [9, 10 & 18]. Researchers worldwide categorically pioneered hybrid CMOS SET devices in mobilizing advanced nano realizations [11, 12 & 16, 17].

One such research attempt is being reported here in, this letter. The subsequent section describes the pedagogy of MIB based nibble multiplexer which is unique of its kind & later on the same is being scanned to unearth the rare aspects of hybrid CMOS-SET.

MIB BASED NIBBLE MULTIPLEXER DESIGN AND OPERATION

The authors only to limit themselves within the space and owing to the compactness adhered to the previous work done of Gope.et.al.[19-26] and subsequently renders few basic design specs of hybrid CMOS-SET based MIB models in the below enumerated Fig.1. Ephemeral analytical study is made on the basis of MIB operations. For simplification 4 number of inputs along with 1 individual carry input has been used and the circuit is quite simple although the robustness is uncompromised. Tanner environment has been used to simulate the model and BSIM 4.0 is used categorically for the empirical demonstration of the proposed model.

COMPARATIVE STUDY

Mathematically hybrid CMOS SET is pivotal in designing future electronics. The customary is to design the model using least number of tunnel junctions as well as capacitors so that the minimization is not captivated by the technological limitations. A deep analogy is tendered in the table below for simplification that reckons the comparative

study of propagation delay, power consumption and the number of CMOS/SETs.

Following Table.1 is a comparative study of Power Supply of

Table 1. Power Dissipation of Hybrid CMOS-SET Circuits

Circuit type	Power Supply	No. of MOS	No. of SET
AND Gate	0.01V	3	3
OR Gate	0.01V	3	3
NOT Gate	0.01V	1	1

CONCLUSION

The authors collectively acknowledges the painstaking endeavor in designing this hybrid CMOS-SET made MIB based Nibble Multiplexers. The elementary designs has largely been pondered over to keep the pace with the straight forwardness and so that to have a clear design specs. The circuit configuration ultimately resolves the issue of background charge problem, low gain, room temperature operation. The device produces greater trade off when compared to its conventional counterpart

ACKNOWLEDGEMENTS

Dr. Jayanta Gope, sincerely acknowledges the financial contribution led down by Honorable Director, Camellia School of Engineering and Technology to undertake this research in Nano Device Computing Laboratory.

REFERENCES

[1] A. R. H. Dennard et al., "Design of Micron MOS Switching Devices", presented at the IEEE IntI. Electron Devices Meeting, 6 December, 1972
[2] www.itrs.net/reports.html
[3] Konstantin k. Likharev, “Single- electron device and their applications”, Proc. IEEE Vol. 87, PP. 606-632, April 1999.
[4] Qiaoyan Yu, student member IEEE, “Single-electron devices”, Manuscript received Dec. 12, 2006.
[5] Andreas Scholze, “Simulation of single-electron devices,” Ph.D. dissertation, Univ. of Jena, Germany, 2000.
[6] L .J. Yen, Ahmad Radzi Mat Isa, Karsono Ahmad Dasuki, “Modeling and Simulation of single-electron transistor”, et al. / Journal of Fundamental Science 1 (2005) 1-6.
[7] Amiza Rasmi & Uda Hashim “Single-electron transistor (SET): Literature Review” journal 2005, koieg University, Malaysia.
[8] M. M. Ziegler and M. R. Stan, “A case for CMOS /nano codesign,”
[9] S. Mahapam, A.M. lonescu, K. Banejee, M.J.Declerq, “Modelling and analysis of pow- dissipation in single electron logic”, Technical Digest of lEDM 2002.
[10] S. Mahapatra, A.M. lonescu, K. Baneiee, “A quasi-analytical SET model for few electron circuit simulation”, IEEE Electron De”. Lett.,Vol. 23,No. 6,pp. 366-368,2002.
[11] A. Venkataratnam and A. K. Goel, Design and simulation of logic circuits with hybrid architectures of single electron transistors and conventional devices, 1st Intl. Conf. Nano-Networks and Workshops, 2006. NanoNet ’06, September (2006), pp. 1–5.
[12] H. Inokawa, A. Fujiwara, and Y. Takahashi, A multiple-valued logic with merged single-electron and MOS transistors, Electron Devices Meeting, 2001, IEDM Technical Digest, Intl., December (2001), pp. 721–724.
[13] L. Qin, C. Li, Z. Youjie, W. Gang, and W. Sen, Design and simulation of logic circuits by combined single electron and MOS transistor structures, Proc. IEEE Intl. Conf. Nan/Micro Engineered and Molecular Sys., January (2008).
[14] S. Mahapatra et al., IEEE Trans. Electron Devices 51, 1772 (2004).
[15] S. Mahapatra et al., A CAD framework for co-design and analysis of CMOS-SET hybrid integrated circuits, Proc. of 2003 IEEE.
[16] S.J. Shin, C.S. Jung, B.J. Park, T.K. Yoon, J.J. Lee, S.J. Kim, et al., Appl. Phys. Lett. 97, 103101 (2010).
[17] S.J. Shin, J.J. Lee, H.J. Kang, J.B. Choi, S.R. Eric Yang, Y. Takahashi, et al., Nano Lett. 11, 1591 (2011).
[18] Santanu Mahapatra, Adrian Mihai Ionescu, “Hybrid CMOS Single-Electron-Transistor Device and Circuit Design” Artech House, Inc., ISBN: 1596930691, 2006.
[19] J. Gope et.al. “Empirical Study of Incorporation of SET and Hybrid CMOS-SET in Decision Making Sub-Systems”, International Journal of Science and Research (IJSR), Volume 3 Issue 6, June 2014, pp-2657-2661.

[20] J. Gope et.al. "Analytical Modeling of Hybrid CMOS-SET Based Moore and Mealy Logical Circuit", IPASJ International Journal of Computer Science (IIJCS), Volume 2, Issue 5, May 2014, pp-6-12.
[21] J. Gope et.al. "Implementation of Decision Making Sub-System Using SET and Hybrid CMOS-SET – A Case Study", International Journal of Advanced Research in Computer Science and Software Engineering 4(6), June - 2014, pp. 1085-1090.
[22] J. Gope et.al., "Modelling of Hybrid CMOS-SET based Highly Efficient Parallel-In-Serial-Out Shift Register for Next Generation Electronics", International Journal of Engineering and Management Research, Volume-4, Issue-3, June-2014, pp-46-51.
[23] J. Gope et.al., "Hybrid CMOS-SET Decision Making Nano IC: A Case Study", International Journal of Science, Engineering and Technology Research (IJSETR), Volume 4, Issue 6, June 2015, pp-1767 -1772.
[24] J. Gope et.al. "Implementation of Low Power Consuming Hybrid CMOS-SET Devices for Stair Case Lighting: A Case Study for Decision Making Subsystems", International Journal of Scientific Engineering and Technology Research Volume.04, IssueNo.10, April-2015, Pages: 1878-1881.
[25] J. Gope et.al. "EMPIRICAL DEMONSTRATION OF NEXT GENERATION HIGH SPEED HYBRID CMOS-SET BASED CONSUMER FRIENDLY IBM MACHINE SUBSECTION", International Journal of Engineering Sciences & Research Technology, [Gope, 4(5): May, 2015], pp -439-444.
[26] J. Gope et.al. "Synthesizing of SET Based Indirect Logic Nano IC for Pulse Train Generation", INTERNATIONAL JOURNAL FOR RESEARCH & DEVELOPMENT IN TECHNOLOGY, Volume-4,Issue-2, Aug – 2015, pp1-4.

AUTHOR BIBLIOGRAPHY

	**Dr. Jayanta Gope**, PhD (Engg.), MIEEE & Chartered Engineer has received his PhD Degree in Nanotechnology from Jadavpur University, Kolkata and is presently associated with Camellia School of Engineering and Technology. His field of interest includes Nano device modeling, Single Electronic devices, Spintronic Devices, Hybrid CMOS-SET. He has already published more than 50 International research articles in this category. He is nominated as Editorial Board Member and Reviewer of some esteemed Journals and is guiding 4 PhD Scholars in the field of Nanotechnology. He is a life Member of 'CE'& 'ISCA'.
	**Mr. Deep Mukherjee** is a final year student of B.Tech in Electronics and Communication Engineering Department of Camellia School of Engineering and Technology, West Bengal, India.
	**Mr. Arijeet Kushari** is a final year student of B.Tech in Electronics and Communication Engineering Department of Camellia School of Engineering and Technology, West Bengal, India.
	**Ms. Mahuya Panda**,(M.E, IIEST, Shibpur) is presently coordinating as HOD in the Dept of EE & EEE in Camellia School of Engineering and Technology. She is also pursuing PhD in University of Kalyani.

ISSN: 2277-9655
(I2OR), Publication Impact Factor: 3.785

Figure:

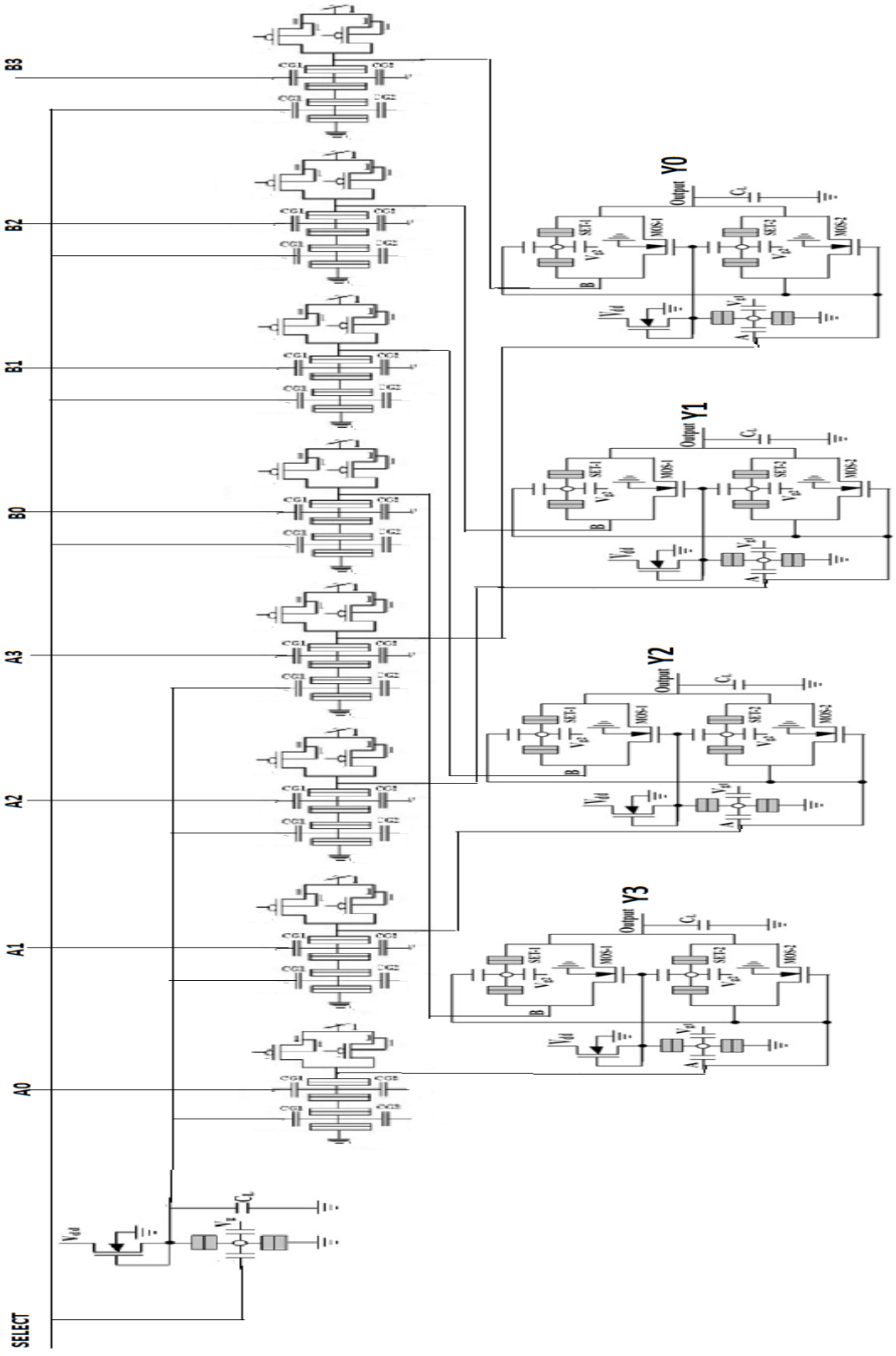

Fig.1 Hybrid CMOS SET made MIB model based 4 input Nibble Multiplexer